WHAT IS CLAIMED IS:

1. A semiconductor device, comprising a surge protection circuit electrically connected to a signal input terminal and having a first transistor and a second transistor; wherein

the semiconductor device is configured such that said first transistor is more susceptible to breakdown than said second transistor, by implementing such a configuration that a narrowest region of a base of said first transistor has a width different from a narrowest region of a base of said second transistor.

2. The semiconductor device according to claim 1, configured such that said first transistor is more susceptible to breakdown than said second transistor, by implementing such a configuration that a region attaining a function as said base of said first transistor has an impurity density different from a region attaining a function as said base of said second transistor.

3. The semiconductor device according to claim 1, wherein

the narrowest region of said base of said first transistor has a width smaller than the narrowest region of said base of said second transistor.

4. The semiconductor device according to claim 1, wherein

in said surge protection circuit, a collector of said first transistor and a collector of said second transistor are electrically connected to said signal input terminal, said base of said first transistor and said base of said second transistor are formed so as to have a same conductivity type, and are electrically connected to each other, and an emitter of said first transistor is electrically connected to said base of said first transistor and said base of said second transistor.

5. The semiconductor device according to claim 1, wherein

said surge protection circuit further includes a resistance element,

an emitter of said second transistor and one end of said resistance element are electrically connected to said signal input terminal, said base of said first transistor and a collector of said second transistor are formed so as to have a same conductivity type, and are electrically connected to each other, an emitter of said first transistor is electrically connected to said base of said first transistor and said collector of said second transistor, and a collector of said first transistor is electrically connected to said base of said second transistor and another end of said resistance element.

6. The semiconductor device according to claim 1, wherein

said surge protection circuit further includes resistance element, the emitter of said second transistor and one end of said resistance element are electrically connected to said signal input terminal, said base of said first transistor and said base of said second transistor are formed so as to have a same conductivity type, and are electrically connected to each other, an emitter of said first transistor is electrically connected to said base of said first transistor, said base of said second transistor, and another end of said resistance element, and a collector of said first transistor is electrically connected to a collector of said second transistor.

7. A semiconductor device, comprising a surge protection circuit electrically connected to a signal input terminal and having a first transistor and a second transistor; wherein

the semiconductor device is configured such that said first transistor is more susceptible to breakdown than said second transistor, by implementing such a configuration that a region attaining a function as a base of said first transistor has an impurity density different from that of a region attaining a function as a base of said second transistor.

8. The semiconductor device according to claim 7, wherein

the region attaining a function as said base of said first transistor has an impurity density higher than that of the region attaining a function as said base of said second transistor.

9. A semiconductor device with a surge protection circuit electrically connected to a signal input terminal and having a first transistor and a second transistor, comprising:

a semiconductor substrate having a main surface; and

a field oxide film formed on the main surface of said semiconductor substrate; wherein

an emitter of said first transistor and a collector of said second transistor are electrically connected to said signal input terminal,

a collector of said first transistor and a base of said second transistor are formed so as to have a same conductivity type, and are electrically connected to each other,

a base of said first transistor is electrically connected to said emitter of said first transistor and said collector of said second transistor, and

a pn junction of said emitter and said base of said first transistor is in contact with one end of said field oxide film, and a pn junction of said collector and said base is in contact with another end of said field oxide film.